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(Not for submission under 37 CFR 1.99)

Application Number		09901930
Filing Date		2001-07-09
First Named Inventor	Jae-Yoon SIM	
Art Unit	2816	
Examiner Name	My Team Lead Wells	
Attorney Docket Number	9898-204	

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KW	1	TANAKA, HITOSHI, et al., A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme, IEEE Journal of Solid-State Circuits, August, 1999, pp. 1084-1090, Vol. 34, No. 8	<input type="checkbox"/>

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Examiner Signature	Kenneth M Wells	Date Considered	9/17/07
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PATENT APPLICATION
Docket No. 9898-204
Client No. SS-16038-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jae-Yoon Sim and Jei-Hwan Yoo
Serial No. 09/901,930 Examiner: Wells
Conf. No. 7100 ~~Terry D. Cunningham~~
Filed: July 9, 2001 Art Unit: 2816
For: NEGATIVE VOLTAGE GENERATOR FOR A SEMICONDUCTOR
MEMORY DEVICE

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

FOREIGN PATENT DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Application</u> <u>Number</u>	<u>Filing date</u> <u>Date</u>	<u>Country</u>	<u>Name</u>
<u>KHW</u>		94020909	August 24, 1994	Korea	

OTHER DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Author, Title, Date, Pertinent Pages, Etc.</u>
<u>KHW</u>		English Language Abstract of Korean Application No: 94020909, 8/24/94.

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